

10V Drive Nch MOS FET

RDN100N20

●Structure

Silicon N-channel
MOS FET

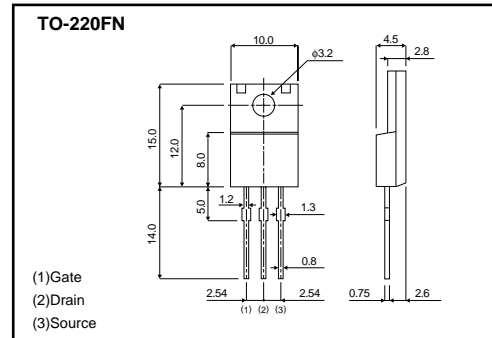
●Features

- 1) Low on-resistance.
- 2) Low input capacitance.
- 3) Excellent resistance to damage from static electricity.

●Application

Switching

●External dimensions (Unit : mm)



●Packaging specifications

Type	Package	Bulk
	Code	-
	Basic ordering unit (pieces)	500
RDN100N20		○

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	200	V
Gate-Source Voltage	V_{GSS}	±30	V
Drain Current	Continuous	I_D	10 A
	Pulsed	I_{DP} *1	40 A
Reverse Drain Current	Continuous	I_{DR}	10 A
	Pulsed	I_{DRP} *1	40 A
Source Current (Body Diode)	Continuous	I_S	10 A
	Pulsed	I_{SP} *1	40 A
Avalanche Current	I_{AS} *2	10	A
Avalanche Energy	E_{AS} *2	120	mJ
Total Power Dissipation (Tc=25°C)	P_D	35	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

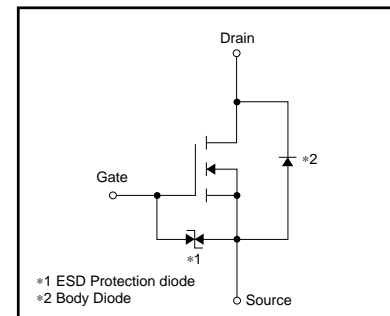
*1 $P_W \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 $L = 1.8mH$, $V_{DD} = 50V$, $R_G = 25\Omega$, 1Pulse, $T_{ch} = 25^\circ C$

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to case	$R_{th(ch-c)}$	3.57	°C/W
Channel to ambient	$R_{th(ch-a)}$	62.5	°C/W

●Equivalent circuit



*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	$V_{GS}=\pm 30V, V_{DS}=0V$
Drain-Source Breakdown Voltage	$V_{(BR) DSS}$	200	—	—	V	$I_D=250\mu A, V_{GS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	25	μA	$V_{DS}=200V, V_{GS}=0V$
Gate Threshold Voltage	$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS}=10V, I_D=1mA$
Static Drain-Source On-State Resistance	$R_{DS(on)}^*$	—	0.27	0.36	Ω	$I_D=5A, V_{GS}=10V$
Forward Transfer Admittance	$ Y_{fs} ^*$	2.3	3.8	—	S	$V_{DS}=10V, I_D=5A$
Input Capacitance	C_{iss}	—	543	—	pF	$V_{DS}=10V$
Output Capacitance	C_{oss}	—	193	—	pF	$V_{GS}=0V$
Reverse Transfer Capacitance	C_{rss}	—	64	—	pF	$f=1MHz$
Turn-On Delay Time	$t_{d(on)}^*$	—	13	—	ns	$I_D=5A, V_{DD} \approx 100V$
Rise Time	t_r^*	—	29	—	ns	$V_{GS}=10V$
Turn-Off Delay Time	$t_{d(off)}^*$	—	38	—	ns	$R_L=20\Omega$
Fall Time	t_f^*	—	26	—	ns	$R_G=10\Omega$
Total Gate Charge	Q_g^*	—	15.0	30.0	nC	$V_{DD}=100V$
Gate-Source Charge	Q_{gs}^*	—	5.0	—	nC	$V_{GS}=10V$
Gate-Drain Charge	Q_{gd}^*	—	5.2	—	nC	$I_D=10A$

* Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}^*	—	—	2.0	V	$I_S=5A, V_{GS}=0V$
Reverse recovery time	t_{rr}^*	—	133	—	ns	$I_{DR}=10A, V_{GS}=0V$
Reverse recovery charge	Q_{rr}^*	—	0.54	—	μC	$di/dt=100A/\mu s$

* Pulsed

Transistors

●Electrical characteristic curves

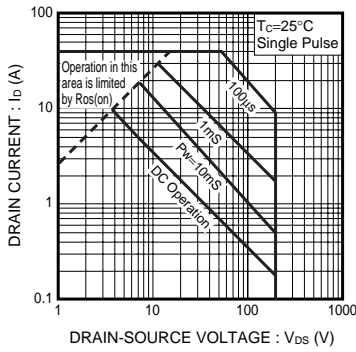


Fig.1 Maximum Safe Operating Area

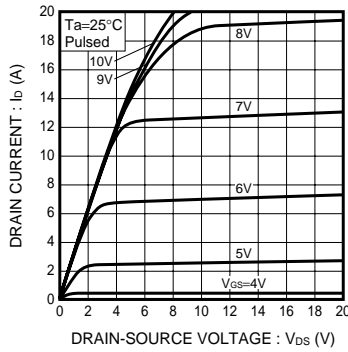


Fig.2 Typical Output Characteristics

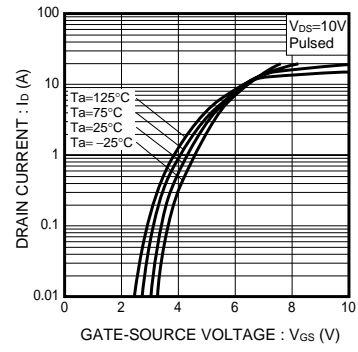


Fig.3 Typical Transfer Characteristics

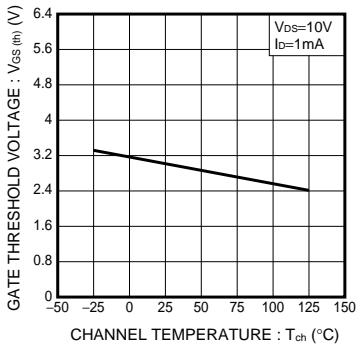


Fig.4 Gate Threshold Voltage vs. Channel Temperature

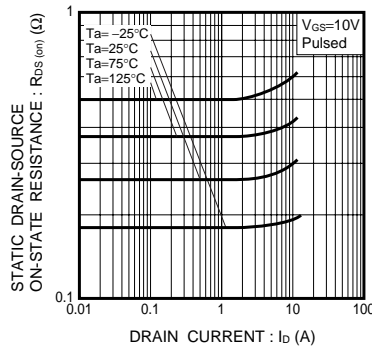


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

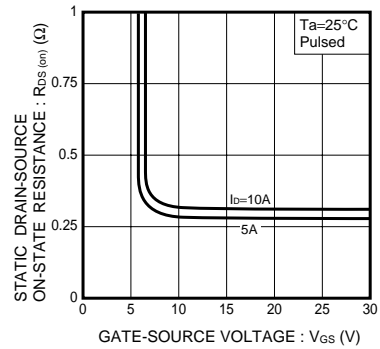


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

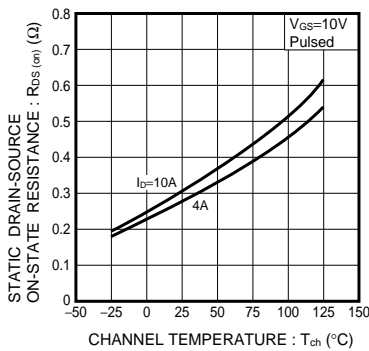


Fig.7 Static Drain-Source On-State Resistance vs. Channel Temperature

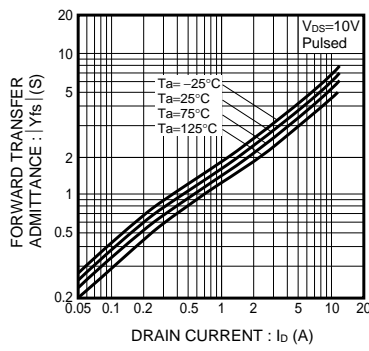


Fig.8 Forward Transfer Admittance vs. Drain Current

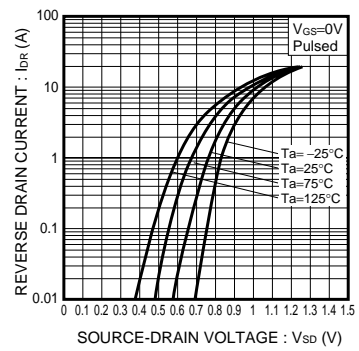


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

Transistors

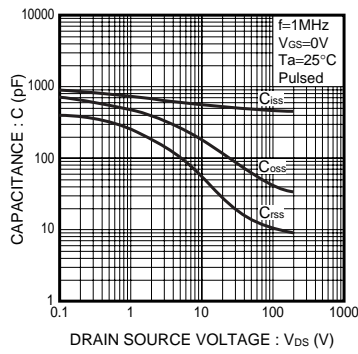


Fig.10 Typical Capacitance vs. Drain-Source Voltage

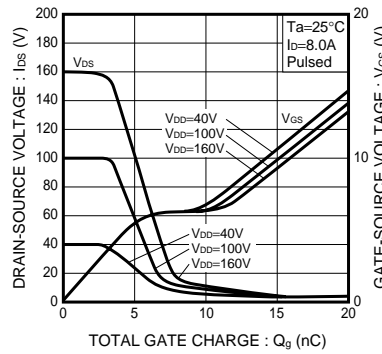


Fig.11 Dynamic Input Characteristics

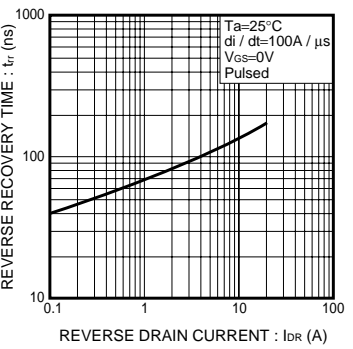


Fig.12 Reverse Recovery Time vs. Reverse Drain Current

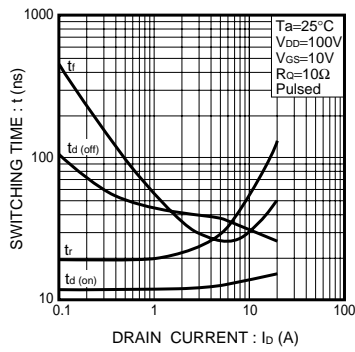


Fig.13 Switching Characteristics

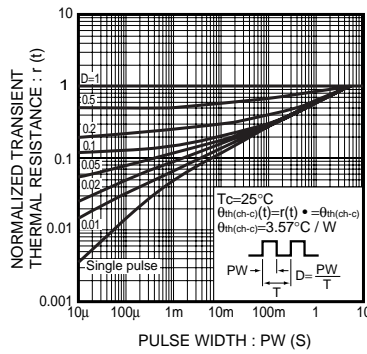


Fig.14 Normalized Transient Thermal Resistance vs. Pulse Width

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